UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,680	12/11/2003	Donald W. Plass	POU920030171US1	8960

7590 08/26/2005

Andrew J. Wojnicki, Jr.
Intellectual Property Law
IBM Corporation, MS P386
2455 South Road
Poughkeepsie, NY 12601

EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,680	PLASS ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 and 16-20 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,489,658 to Richter et al.

Regarding to claim 1, Richter discloses an insulated gate field effect transistor, comprising a source 13, a drain 12, and channel 6 formed in a layer of a single-crystal semiconductor 2, said layer disposed over and insulated from a bulk semiconductor layer of a substrate by a buried insulator layer, a gate conductor 3 disposed in an annular pattern overlying said channel 6, such that said gate conductor 3 surrounds one of said source 13 and said drain 12 disposed to the inside of said annular pattern, the other of said source 13 and said drain 12 being disposed to the outside of said annular pattern, said gate conductor 3 further including a second pattern 9 connected to said annular pattern, and a conductive body contact (col. 3, lines 7-8) to said single-crystal semiconductor layer disposed in the vicinity of said second pattern (col. 2, lines 50-67, col. 3, lines 1-8, and fig. 4).

Regarding to claim 2, the insulated gate field effect transistor, wherein said source, drain and channel region are disposed in an active area of said layer bounded by one or more isolation structures (col. 2, lines 50-59).

Regarding to claim 3, the insulated gate field effect transistor wherein said second pattern extends linearly between said annular pattern and an edge of said active area (fig. 4).

Regarding to claim 4, the insulated gate field elect transistor, wherein said annular pattern includes a pair of parallel portions oriented in a first direction substantially parallel to an edge of said active area and further includes angled portions oriented at an angle to said first direction (fig. 4).

Regarding to claim 5, the insulated gate field effect transistor, wherein at least some of said angled portions are oriented at angles between about 30 degrees and 60 degrees with respect to said first direction (fig. 1).

Regarding to claim 6, the insulated gate field elect transistor, wherein at least some of said angled portions are oriented at angles of about 45 degrees (fig. 4).

Regarding to claim 7, the insulated gate field effect transistor, wherein said transistor is an n-type FET, the source is disposed to the outside of the annular pattern, and the body contact is disposed on a region of said layer adjacent to said source (fig. 4).

Regarding to claims 16-20, Richter discloses a method of making an insulated gate field effect transistor comprising providing a substrate 2 having a single-crystal semiconductor layer separated from a bulk semiconductor portion by a buried insulator layer, forming a source 13, a drain 12, and a channel 6 in said single-crystal semiconductor layer, forming a gate conductor 3 disposed in an annular pattern overlying said channel, such that said gate conductor surrounds one of said source and said drain disposed to the inside of said annular pattern, the other of said source and said drain being disposed to the outside of said annular pattern, said gate conductor further including a second pattern 9 connected to said annular pattern, and forming an electrically conductive contact to said single-crystal semiconductor layer in the vicinity of said second pattern (col. 2, lines 50-67, col. 3, lines 1-20, and fig. 4).

Regarding to claim 17, the method wherein said gate conductor is patterned to form said annular pattern and said second pattern prior to depositing at least one material selected from the group consisting of heavily doped polysilicon, metals and metal compounds to form said electrically conductive contact (col. 2, lines 63-67, col. 3, lines 1-8).

Regarding to claim 18, the method wherein said material is deposited prior to implanting ions to form said source, and said drain, said channel remaining as an area disposed under at least portions of said gate conductor between said source and said drain (col. 2, lines 63-67, col. 3, lines 1-8).

Regarding to claim 19, the method further comprising patterning an active area in said single-crystal semiconductor Iayer; providing trench isolations to isolate said active area, wherein said source, said drain, and said channel are formed in said active area (col. 2, lines 63-67, col. 3 and col. 4, lines 1-56).

Regarding to claim 20, the method wherein said second pattern extends linearly between said annular pattern and an edge of said active area (fig. 4).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-9 are rejected under 35 U.S.C. 103 (a) as being unpatentable over US patent No. 6,489,658 to Richter et al. in view of U.S. Patent No. 5,689,129 to Pearce.

Regarding to claim 8, Richter discloses the claimed invention except for the insulated gate field effect transistor wherein said gate conductor further includes a third pattern connected to said annular pattern, said second and third patterns extending from first and second locations of said annular pattern in substantially opposite directions.

Pearce discloses the insulated gate field effect transistor wherein said gate conductor further includes a third pattern connected to said annular pattern, said second and third patterns extending from first and second locations of said annular pattern in substantially opposite directions (cols. 1,lines 60-67, cols 2-3 and fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the insulated gate field effect transistor wherein said gate conductor further includes a third pattern connected to said annular pattern, said second and third patterns extending from first and second locations of said annular pattern in substantially opposite directions, as taught by Pearce in order to design the power MOS switches with low resistance with crucial to the price competitiveness of the MOS process and to increase the specific channel width density of an MOS transistor array that lead to improved efficiency of the device (col. 1, lines 13-23).

Regarding to claim 9, Pearce discloses the insulated gate field effect transistor, wherein said second and said third patterns extend linearly between said annular pattern and edges of said active area (fig. 3).

Claims 10-15 are rejected under 35 U.S.C. 103 (a) as being unpatentable over US patent No. 6,489,658 to Richter et al. in view of the remark.

Regarding to claims 10-15, Richter discloses the insulated gate field effect transistor, comprising a source 13, a drain 12, and channel 6 formed in a layer of a single-crystal semiconductor 2, said layer disposed over and insulated from a bulk semiconductor substrate by a buried insulator layer 4 (cols. 2-3, and fig. 4). Richter does not disclose a gate conductor including a first multiple finger pattern overlying said channel and a second multiple finger pattern overlying said channel, and a connecting pattern conductively connecting said first and second multiple finger patterns, and an electrically conductive body contact to said single-crystal semiconductor layer disposed in the vicinity of said connecting pattern.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a gate conductor including a first multiple finger pattern overlying said channel and a second multiple finger pattern overlying said channel, and a connecting pattern conductively connecting said first and second multiple finger patterns, and an electrically conductive body contact to said single-crystal semiconductor layer

disposed in the vicinity of said connecting pattern, since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran